In the Specification

Please amend the Specification as follows:

[0053]

~~[0049]~~ The method can be easily extended to multiple reset pulses in order to provide an arbitrary output versus illumination characteristic in a monotonically increasing piecewise linear fashion. Referring also to Figure 7, a multiple reset pulses, $V_R(t)$, is applied to the gate **21** of a reset transistor **19** of the pixel over the course of an exposure period. The spacing between the reset pulses and the height of individual reset pulses determine the compression characteristic. The height of the reset pulses get progressively lower over the course of an integration period. It is also noted that the train of progressively decreasing intra-period reset pulses can progressively decrease in pulse width. While this reset node is shown in this example as a MOS transistor gate, it is to be recognized that other reset node configurations can be accommodated by the control technique of the present invention.

LR 5/30/08